## ABSTRACT OF THE DISCLOSURE

[0063] This invention reduces the scale of a Huffman table used for decoding. A queuing unit queues a variable-length code word from a received bitstream. A switch circuit discriminates the type of the code word in accordance with the pattern of a predetermined number of bits at the start of the queued variable-length code word, extracts data having a sufficient code word length from a predetermined bit position on the basis of the discrimination result, and outputs the result to a Huffman table. The Huffman table compares the data from the switch circuit with a variable-length code word stored in advance, and when the data and the variable-length code word coincide, outputs first symbol data. The Huffman table also generates a sum value for the first symbol data, and generates two second symbols from the sum result. A selection unit selects and outputs one of the first symbol and two second symbols in accordance with the type of the received code. A selection unit selects and outputs one of the symbol selected by the selection unit and a symbol from an FLC decoder on the basis of the data queued by the queuing unit.

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